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Paper 10
Entered: April 3, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2017-00114
Patent 7,206,978 B2

Before SALLY C. MEDLEY, BARBARA A. PARVIS, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1–6 and 8–14 of U.S. Patent No. 7,206,978 B2

(Ex. 1001, "the '978 patent"). Paper 2 ("Pet."). Polaris Innovations Ltd. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108. Upon consideration of the Petition and Preliminary Response, we conclude Petitioner demonstrates a reasonable likelihood of prevailing in demonstrating the unpatentability of claims 1, 6, 8–11, 13, and 14 of the '978 Patent, but does not demonstrate a reasonable likelihood of prevailing in showing the unpatentability of claims 2–5 and 12. Accordingly, we institute an *inter partes* review as to only claims 1, 6, 8–11, 13, and 14 of the '978 Patent on the grounds specified below.

A. Related Matters

The parties state that the '978 Patent is the subject of a pending lawsuit in the Central District of California, i.e., *Polaris Innovations Ltd. v. Kingston Tech. Co.*, Case No. 8:16–cv-300 (C.D. Cal.)[1] and the lawsuit includes assertions against Petitioner. Pet. 1; Paper 3 (Patent Owner's Mandatory Notices), 1.

B. The '978 Patent

The '978 Patent is directed to error detection in a circuit module. Ex. 1001, 1:7–8. Figure 3 of the '978 Patent is reproduced below.

[1] This lawsuit is referred to herein as the "companion district court lawsuit."

FIG 3

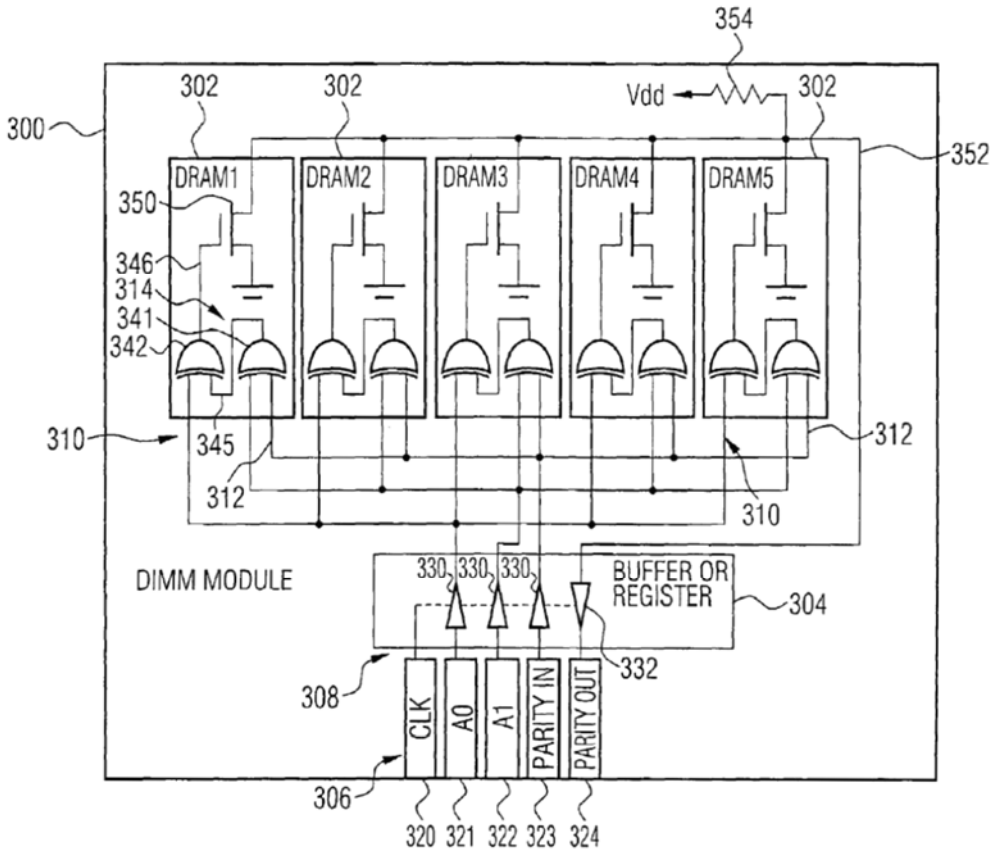

Figure 3 illustrates a schematic view of a memory module.

As shown in Figure 3 above, each of dynamic random access memory (DRAM) chips 302 on module board 300 is connected to one of sub-buses 310. *Id.* at 4:43–49. An indication signal generating unit 314 is embedded in each memory chip 302. *Id.* at 4:51–52. Clock, address, check, and error signals are received from the motherboard by terminals 320–324 in connector portion 306 (*id.* at 4:53–60), which is connected to buffer 304 via module main bus 308 (*id.* at 4:45–46).

Indication signal generating unit 314 includes two exclusive OR (XOR) gates 341 and 342. *Id.* at 5:16–17. Indication signal generating unit 314 receives command and address bits and the check signal. *Id.* at 5:18–26.

Indication signal generating unit 314 outputs indication signal 346. *Id.* at 5:26–28.

C. Illustrative Claim

Petitioner challenges claims 1–6 and 8–14 of the '978 Patent. Claims 1 and 13 are independent claims. Claims 2–6, 8–12, and 14 depend, directly or indirectly, from claims 1 or 13. Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A circuit module comprising:
>
> a module board;
>
> a plurality of circuit units arranged on the module board, each circuit unit consisting of a single integrated circuit memory chip;
>
> a main bus having a plurality of lines, branching into a plurality of sub-buses having a plurality of lines, each of the sub-busses being connected to one of the plurality of circuit units;
>
> wherein each circuit unit comprises an indication signal generating unit for providing an indication signal based on a combination of the signals received on the plurality of lines of the sub-bus connected to the respective circuit unit, and an indication signal output for outputting the indication signal.

Id. at 7:30–44.

D. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–6 and 8–14 are unpatentable based on the following grounds (Pet. 10–12):

Reference(s)	Basis	Challenged Claim(s)
Humphrey[2] alone or in combination with Admitted Prior Art[3]	§ 103(a)	1–3, 6, 8, and 10–14
Humphrey, Admitted Prior Art, and Cromer[4]	§ 103(a)	9
Humphrey, Admitted Prior Art, and Majni[5]	§ 103(a)	4 and 5
Raynham[6] and Seyyedy[7]	§ 103(a)	1–3, 10, 11, 13, and 14
Raynham, Seyyedy, and Humphrey	§ 103(a)	6
Raynham, Seyyedy, and Admitted Prior Art	§ 103(a)	8
Raynham, Seyyedy, and Cromer	§ 103(a)	9

As support, Petitioner proffers a Declaration of Dr. Vivek Subramanian, who has been retained by Petitioner for the instant proceeding. Ex. 1003 ¶¶ 1–3.

II. DISCUSSION

A. Overview

A patent claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole,

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[2] European Patent Application 0 084 460 A2, published July 27, 1983 (Ex. 1008) ("Humphrey").
[3] Admitted Prior Art (i.e., Ex. 1001, 1:11–38, 1:41–43, 1:57–59, Figs. 1, 2 (cited in Pet. 15–18, 22, 23)).
[4] European Patent Application EP 1 029 326 B1, published Aug. 23, 2000 (Ex. 1007) ("Cromer").
[5] U.S. Patent No. 7,028,213 B2, issued Apr. 11, 2006 (Ex. 1011) ("Majni").
[6] U.S. Patent No. 5,127,014, issued June 30, 1992 (Ex. 1005) ("Raynham").
[7] U.S. Patent No. 6,282,689 B1, issued Aug. 28, 2001 (Ex. 1009) ("Seyyedy").

would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. 35 U.S.C. § 103(a). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). In that regard, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

B. Person of Ordinary Skill in the Art

Petitioner proposes that a person of ordinary skill in the art had a Master's degree in Electrical Engineering and at least 2 years' experience working in the field of semiconductor memory design. Ex. 1003 ¶¶ 17–19 (cited *e.g.*, in Pet. 20, 22). Patent Owner does not dispute Petitioner's proposal. *See generally* Prelim. Resp.

We also consider the level of skill implied by the disclosures of the prior art references. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself can reflect the appropriate level of skill in the art). Additionally, this person is of ordinary creativity, not an automaton. *KSR*, 550 U.S. at 421.

C. Claim Construction

Petitioner does not identify terms for construction. Pet. 12. Instead, Petitioner contends that it applies the broadest reasonable interpretation to all claim terms and provides further details of how the claims are being interpreted in relevant sections below. *Id.* Petitioner also "expressly reserves the right to advance different constructions" in the companion district court lawsuit. *Id.* n.1.

Patent Owner makes two arguments in response: (1) the Petition fails to identify the function and structure for limitations that are presumed by law to be means-plus-function (Prelim. Resp. 1–4, 6–22); and (2) Petitioner should be held to its previous arguments in the companion district court lawsuit that "indication signal generating unit" is a means-plus-function limitation (*id.* at 1, 8). We address Patent Owner's arguments below.

1. Means-Plus-Function Limitations

We turn to Patent Owner's argument that the Petition fails to identify the function and structure for limitations that are presumed by law to be means-plus-function. Prelim. Resp. 1–4, 6–22. As Petitioner correctly contends (Pet. 12), in an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). We, however, agree with Patent Owner (Prelim. Resp. 9) that several of the challenged claims, i.e., claims 2–5 and 12, include limitations with the language "means" or "means for" and therefore are presumed to

invoke 35 U.S.C. § 112 ¶ 6.[8] *See Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015) (en banc in relevant part) ("use of the word 'means' creates a presumption that § 112, ¶ 6 applies."); *see also In re Donaldson Co.*, 16 F.3d 1189, 1193 (Fed. Cir. 1994) ("[P]aragraph six applies regardless of the context in which the interpretation of means-plus-function language arises, i.e., whether as part of a patentability determination in the PTO or as part of a validity or infringement determination in a court.").

The sixth paragraph of 35 U.S.C. § 112 provides that "[a]n element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." Where a challenged claim contains a means-plus-function limitation under 35 U.S.C. § 112, sixth paragraph, the Petitioner "must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function." 37 C.F.R. § 42.104(b)(3).

Petitioner does not provide any rebuttal to the presumption that § 112, ¶ 6 applies to the means-plus-function limitations recited in claims 2–5 and

[8] Section 4(c) of the Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA") re-designated 35 U.S.C. § 112 ¶ 6, as 35 U.S.C. § 112(f). Because the '978 Patent has a filing date before September 16, 2012, the effective date of § 4(c) of the AIA, we will refer to the pre-AIA version of 35 U.S.C. § 112.

12. Pet. 12.[9] Furthermore, Petitioner does not discuss 35 U.S.C. § 112, ¶ 6 and does not identify what structure in the Specification it believes corresponds to the means-plus-function limitations of claims 2–5 and 12. *See, e.g.*, Pet. 12. Indeed, Petitioner's discussion of the asserted art in relation to claims 2–5 and 12 does not address any corresponding structure in the Specification of the '978 Patent. Pet. 27, 28, 38, 39, 52, 53, 66.

For the reasons given, we agree with Patent Owner that Petitioner has failed to satisfy the identification requirement of 37 C.F.R. § 42.104(b)(3) with regard to the means-plus-function elements of claims 2–5 and 12.

2. "an indication signal generating unit"

We turn to Patent Owner's contention that Petitioner should be held to its previous arguments in the companion district court lawsuit that "indication signal generating unit" is a means-plus-function limitation. Prelim. Resp. 1, 8. Patent Owner, more specifically, contends that deficiencies exist in the Petition similar to those discussed above and, therefore, Petitioner also has failed to satisfy the identification requirement of 37 C.F.R. § 42.104(b)(3) with regard to "an indication signal generating unit." *Id*. at 1–4, 6–22.

Each of the independent claims 1 and 13 recites "an indication signal generating unit." In the instant proceeding, neither party contends that the independent claims include limitations that recite "means" or "means for," or contends that 35 U.S.C. § 112, ¶ 6 should apply to "an indication signal generating unit." Pet. 12; Prelim. Resp. 1–4, 6–22. Furthermore, Patent

[9] Patent Owner contends that the parties agree in the companion district court lawsuit that 35 U.S.C. § 112, ¶ 6 applies. Prelim. Resp. 6.

Owner does not contend that the parties agreed in the companion district court lawsuit that "indication signal generating unit" is a means-plus-function limitation. *Id.* Patent Owner also has not provided as exhibits evidence of the parties' claim construction contentions or a claim construction decision in the companion district court lawsuit. *Id.*

Based on the record before us at this juncture of the proceeding, we are not persuaded that Petitioner should be held to any previous arguments in the companion district court lawsuit regarding the term "indication signal generating unit." We determine that it is not necessary to provide an express interpretation of "an indication signal generating unit." *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) ("[C]laim terms need only be construed 'to the extent necessary to resolve the controversy'") (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Evidentiary Weight of Declaration Evidence

In addition to the asserted prior art, the Petition relies upon Dr. Subramanian's Declaration (Ex. 1003). Patent Owner contends that we should accord Dr. Subramanian's testimony no evidentiary weight because he "simply parrots the Petition" in an attempt to give Petitioner's arguments enhanced probative value. Prelim. Resp. 23. Patent Owner provides an exemplary comparison of the Petition and Dr. Subramanian's Declaration (*id.* at 23–26) and submits a table with additional comparisons (Ex. 2001).

Based on the record before us and at this juncture, we decline to disregard the Declaration (Ex. 1003) as Patent Owner suggests. At this juncture, we are not convinced that similarities in the Petition and Dr. Subramanian's Declaration necessarily indicate that the Declaration is a

copy of an attorney-prepared Petition. Instead, the Petition may be a copy of the Declaration or Dr. Subramanian may have worked with the attorneys to prepare both the Petition and Declaration simultaneously.

E. Dependent Claims 2–5 and 12

For the reasons discussed above with respect to claim construction, we determine that Petitioner has failed to satisfy the identification requirement of 37 C.F.R. § 42.104(b)(3) with regard to the two means-plus-function elements of claims 2–5 and 12. As a threshold matter, to challenge the patentability of a claim including a means-plus-function limitation as obvious under 35 U.S.C. § 103, a petition must identify the specific portions of the specification that describe the structure corresponding to the claimed function and specify where that structure is found in the cited prior art patents or printed publications. 37 C.F.R. §§ 42.104(b)(3), (4). We agree with Patent Owner that because Petitioner does not identify sufficiently any corresponding structure for the above means-plus-function limitations in claims 2–5 and 12, Petitioner has failed to show a reasonable likelihood that it would prevail in establishing unpatentability of claims 2–5 and 12 on any alleged ground.

F. Obviousness of Claims 1, 6, 8–11, 13, and 14 over Humphrey alone or with other art

Petitioner contends claims 1, 6, 8–11, 13, and 14 are unpatentable, under 35 U.S.C. § 103(a), as obvious over Humphrey alone or with other art. Pet. 13–39. Relying on the testimony of Dr. Subramanian, Petitioner explains how Humphrey alone or with the other art teaches all of the claim limitations and provides a reason to combine. *Id.* (citing Ex. 1003).

Petitioner identifies portions of the Background of the Invention of the '978 Patent as Admitted Prior Art (*see, e.g.*, Ex. 1001, 1:11–38, 1:41–43, 1:57–59, Figs. 1, 2 (cited in Pet. 15–18, 22, 23, 30)) and discusses these portions in its analysis of the challenged claims.

1. Overview of Humphrey

Humphrey is directed to detecting errors in a computer memory system. Ex. 1008, Abstract. Figure 1 of Humphrey is reproduced below.

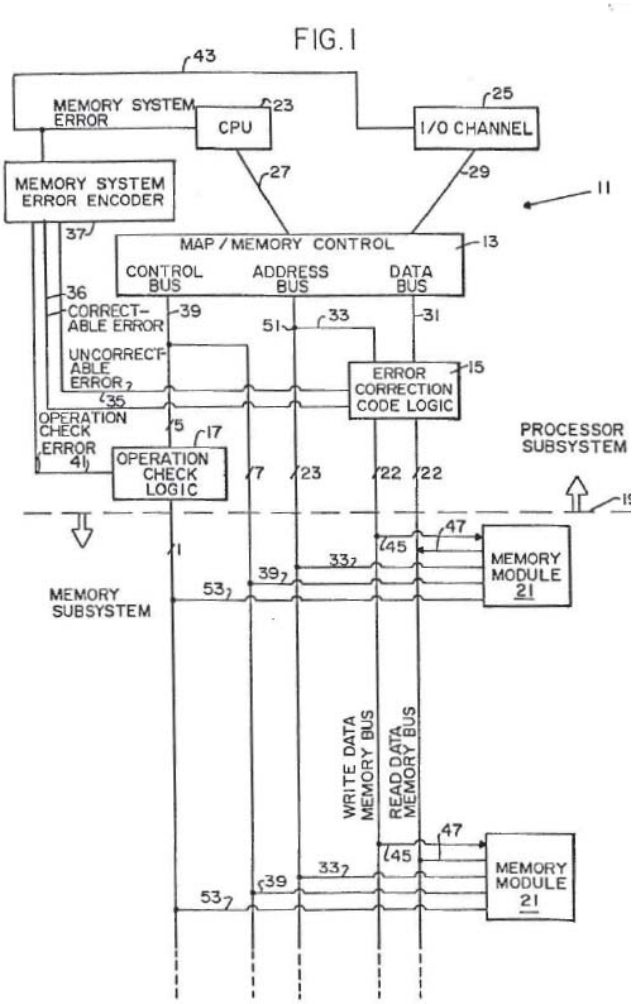

Figure 1 is block diagram of a memory system.

As shown in Figure 1 above, memory system 11 includes a processor subsystem and a memory subsystem. *Id.* at 7:23–33. The processor subsystem includes map/memory control 13 (*id.* at 7:23–25), which is connected by bus 27 to central processing unit (CPU) 23 (*id.* at 7:34–35) and by bus 29 to I/O channel 25 (*id.* at 8:1–4). The memory subsystem includes memory modules 21. *Id.* at 7:29–31. Each memory module 21 has five bus connections, including write and read data buses 45 and 47, address bus 33, and control bus 39. *Id.* at 8:28–9:8.

Figure 2 is reproduced below.

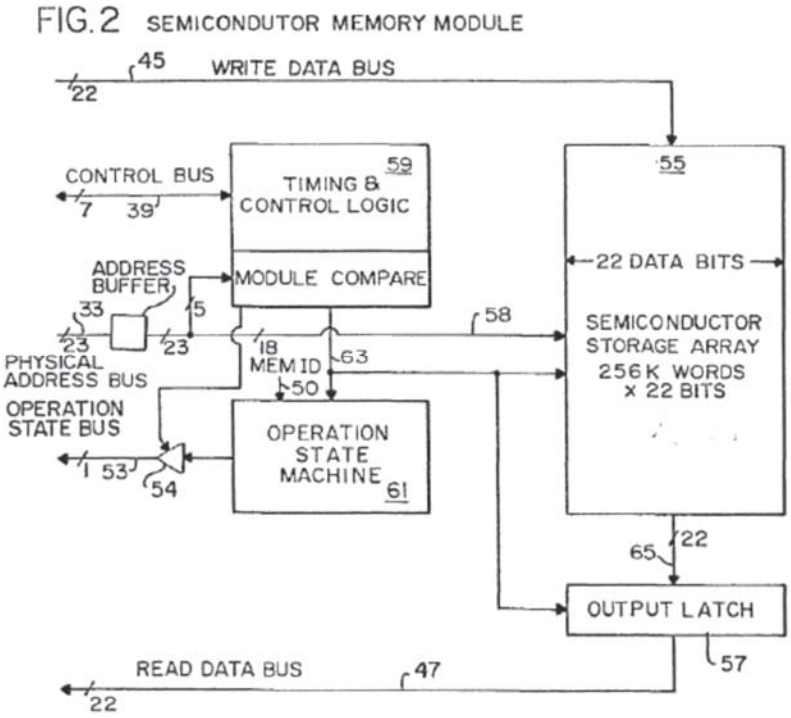

Figure 2 is a block diagram of the memory module portion of the memory system.

As illustrated in Figure 2 above, memory module 21 stores data in semiconductor storage array 55. *Id.* at 10:26–30. Memory module 21 also checks its operations using operation state machine 61. *Id.* at 10:33–35.

2. Overview of Admitted Prior Art[10]

According to the '978 Patent, a conventional structure of computer main memory systems includes a memory controller, a main memory bus and memory chips, such as DRAM chips, that are arranged on memory modules, such as duals in-line memory modules (DIMMs). Ex. 1001, 1:11–16. Figure 1 of the '978 Patent is reproduced below.

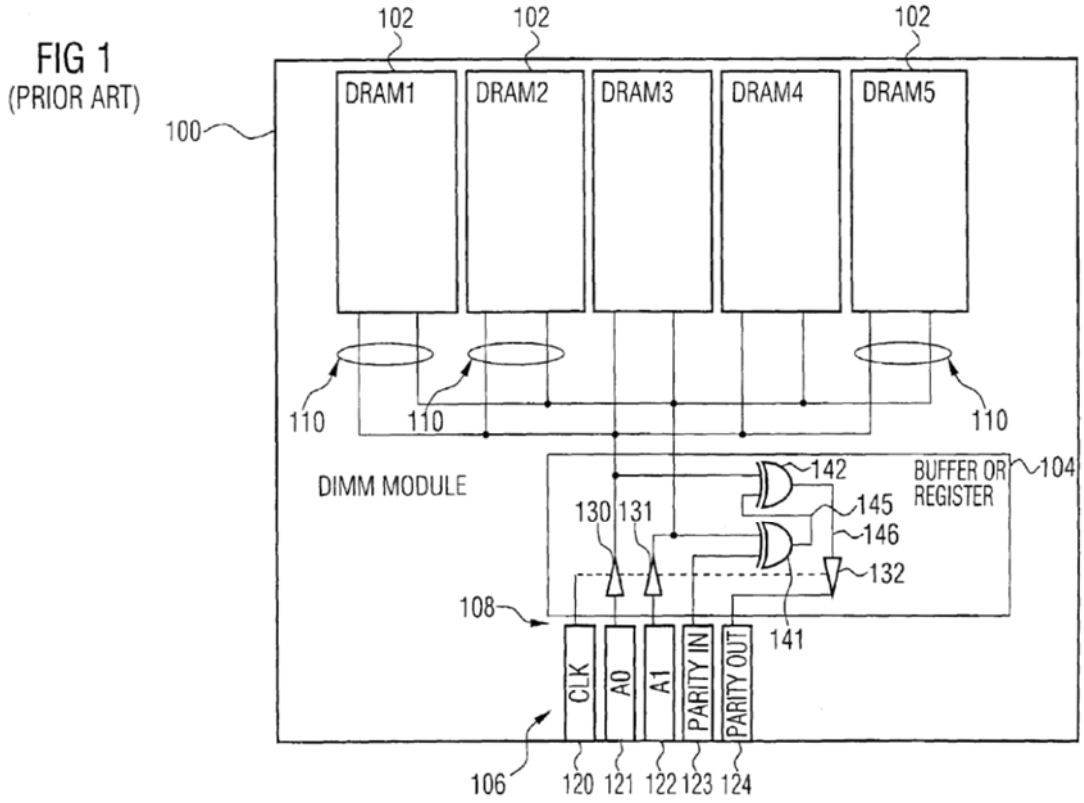

Figure 1 of the '978 Patent is labeled "PRIOR ART" and illustrates DRAM memory chips 102 on module board 100. *Id.* at 1:36–37. As shown

[10] This overview is of portions of the Background of the Invention of the '978 Patent identified by Petitioner as Admitted Prior Art (i.e., Ex. 1001, 1:11–38, 1:41–43, 1:57–59, Figs. 1, 2 (cited in Pet. 15–18, 22, 23)).

in Figure 1, clock, address, check, and error signals are received from the motherboard by terminals 120–124 in connector portion 106 (*id.* at 1:43–51), which is connected to buffer 104 via module main bus 108 (*id.* at 1:38–40). Module main bus 108 branches into sub-buses 110, each of which is connected to one of memory chips 102. *Id.* at 1:41–43.

3. Overview of Cromer

Cromer is directed to providing access protection in memory devices. Ex. 1007 ¶ 1. One such memory device has a memory array and access logic to control access to the memory array. *Id.* ¶ 8. The serial interface of the memory device includes a set of sticky bits 104. *Id.* ¶ 11. Sticky bits 104 provide write access control over protection bit stores. *Id.* ¶¶ 15, 16.

4. Whether Admitted Prior Art is Available as a Basis to Institute Review

Petitioner contends that portions of the Background of the Invention of the ’978 Patent are Admitted Prior Art (*see, e.g.*, Ex. 1001, 1:11–38, 1:41–43, 1:57–59, Figs. 1, 2 (cited in Pet. 15–18, 22, 23)) and are conventional. Pet. 15–17. Petitioner points to the ’978 Patent’s description in the “Background of the Invention” of a “conventional structure of computer main memory systems” (*id.* at 15–16 (citing *e.g.*, Ex. 1001, 1:12–16)) and the labeling of Figures 1 and 2 as prior art (*id.* at 17–18). Petitioner further contends that these are admissions and are eligible for consideration. *Id.*

Patent Owner contends that Petitioner failed to show that the relied upon text in the ’978 Patent is available as a basis to institute review. *See, e.g.*, Prelim. Resp. 26. In particular, Patent Owner contends that “[t]he Board has long recognized that an issued patent cannot be a ‘prior art’

'patent or printed publication' against itself for purposes of consideration of a request to reconsider its patentability." *Id.*

Historically, admissions have been considered in proceedings before the U.S. Patent and Trademark Office in making patentability determinations. For instance, in *In re Nomiya*, when the Appellants' patent application included two figures, Figures 1 and 2, that were labeled as "prior art" and described as such in the specification, the CCPA held:

> We see no reason why appellants' representation in their application should not be accepted at face value as admissions that Figs. 1 and 2 may be considered "prior art" for any purpose, including use as evidence of obviousness under § 103. . . . By filing an application containing Figs. 1 and 2, labeled prior art, *ipsissimis verbis*, and statements explanatory thereof appellants have conceded what is to be considered as prior art in determining obviousness of their improvement.

509 F.2d 566, 570–71 (CCPA 1975) (citations and footnote omitted).

Patent Owner contends that, because of "§ 311(b)'s restrictions," the Admitted Prior Art identified by Petitioner cannot constitute prior art as a basis for an *inter partes* review. Prelim. Resp. 28–32. As set forth in 35 U.S.C. § 311(b), a petitioner in an *inter partes* review may request to cancel a claim "only on the basis of prior art consisting of patents or printed publications."

Upon review of the current record and at this juncture, for the reasons set forth below, we determine that Petitioner has shown sufficiently that Humphrey alone teaches all the claim limitations identified in the Petition as being taught by Humphrey or the Admitted Prior Art. We also find that the teachings of the Admitted Prior Art are consistent with Petitioner's contentions thereby providing additional support at this juncture of the proceeding. We further determine that the Admitted Prior Art constitutes

background knowledge that may be imputed to a hypothetical person of ordinary skill in the art for the purposes of an obviousness analysis.

5. Discussion of Claim 1

We begin our analysis with independent claim 1. Petitioner asserts that Humphrey, alone or in combination with the Admitted Prior Art, teaches all elements of claim 1, and Petitioner provides a rationale for combining the teachings of Humphrey and the Admitted Prior Art. Pet. 13–26.

Claim 1 is directed to a circuit module, which comprises circuit units arranged on a module board and a main bus that branches into sub-buses, each of which is connected to one of the circuit units. Ex. 1001, 7:30–38. Petitioner points to Figure 1 of Humphrey and related teachings and provides supporting testimony of Dr. Subramanian. Pet. 13, 14, 20–24 (citing *e.g.*, Ex. 1008, 2:8–14, 4:7–10, 6:30–32, 7:9–11, 7:23–34, 8:28–35, 9:1–3, 15:1–3, 15:6–9, Fig. 1; Ex. 1003 ¶¶ 19, 61–69).

Consistent with Petitioner's contentions (*id.*), Humphrey teaches memory system 11 comprising memory modules 21 which, based on the record before us at this juncture, appear to teach the structure recited in claim 1 (*see, e.g.*, Ex. 1008, Fig. 1). For instance, each memory module 21 comprises a semiconductor storage array, timing and control logic (Ex. 1008, 4:7–8), and has bus connections, including, for example, input (write) data bus 45, output (read) data bus 47, address bus 33, and control bus 39 (*id.* at 8:28–9:9). The aforementioned buses connect each memory module 21 to map memory control 13 (*id.* at 4:9–10, 8:28–30), which is physically located in the processor subsystem portion (*id.* at 7:23–29). Memory system 11 includes dual access via central processor unit (CPU) 23 and input/output (I/O) channel 25. *Id.* at 7:9–8:27, Fig. 1. CPU 23 is connected to map

memory control 13 by bus 27 (*id.* at 7:34–36) and I/O channel 25 is connected to map memory control 13 by bus 29 (*id.* at 8:1–5). The buses comprises lines including, for example, bus 29, which comprises data, logical address, and control lines connecting I/O channel 25 to map/memory control 13. *Id.*

Claim 1 also recites that each circuit unit comprises an indication signal generating unit, which provides an indication signal based on a combination of signals received on the sub-buses. Ex. 1001, 7:39–44. Petitioner points to Humphrey's teachings relating to generating a signal indicating the status of operations of the memory module and provides supporting testimony of Dr. Subramanian. Pet. 24–26 (citing Ex. 1008, 4:13–20, 10:33–35, 11:8–18, Fig. 2; Ex. 1003 ¶¶ 70–73).

Consistent with Petitioner's contentions (*id.*), Humphrey teaches generating a signal in each memory module 21 indicating the status of operation of that memory module (Ex. 1008, 3:17–19). For instance, Humphrey teaches operation state machine 61 generating such a signal. *Id.* at 11:8–11, Fig. 2. Operation state machine 61 generates the status signal using data received on the buses referred to above (e.g., address bus 33 and control bus 39). *Id.* at 8:28–9:9, 10:33–35, 11:8–28, Fig. 2.

Petitioner also provides contentions regarding supplemental teachings of the Admitted Prior Art, as well as reasons to combine the teachings of Humphrey and the Admitted Prior Art. Pet. 13–20 (citing Ex. 1008, Abstract, 2:17–27, 4:7–8, 4:13–20, 7:23–34, Figs. 1, 2; Ex. 1001, 1:11–38, 1:57–59, Figs. 1, 2; Ex. 1005, Abstract; Ex. 1006; Ex. 1003 ¶¶ 28–31, 44–47). For instance, relying on the testimony of Dr. Subramanian, Petitioner contends that the skilled artisan would have had a reason to combine the

teachings of the asserted art to generate a signal in each memory module indicating its operating status to protect against the known problem of operational error of such units. *Id.* at 18–19 (citing Ex. 1008, 2:17–27, 3:17–20; Ex. 1003 ¶¶ 44–47).

Regarding Patent Owner's contentions, our discussion regarding claim construction above addresses Patent Owner's contentions that we should hold Petitioner to its alleged previous arguments in the companion district court lawsuit that "indication signal generating unit" is a means-plus-function limitation (Prelim. Resp. 1, 8). We also discuss above Patent Owner's contentions regarding evidentiary weight to be given to Dr. Subramanian's Declaration (*id.* at 23–26). Patent Owner does not provide further contentions regarding obviousness of claim 1 over Humphrey alone.

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of showing claim 1 to be unpatentable in view of Humphrey alone.[11]

6. Claims 6, 8, 10, 11, 13, and 14

Turning now to independent claim 13 and dependent claims 6, 8, 10, 11, 13, and 14, Petitioner asserts that Humphrey alone or in combination with the Admitted Prior Art teaches all elements of these claims and provides a rationale for combining the teachings of Humphrey and the Admitted Prior Art. Pet. 13–34. Patent Owner does not argue these claims separately, except as otherwise noted herein. Independent claim 13 is

[11] Based on the record before us at this juncture, the teachings of Admitted Prior Art are consistent with Petitioner's contentions and provide further support for Petitioner's contentions with respect to independent claim 1.

similar to claim 1. Based on the record before us and at this juncture, Petitioner has made a sufficient showing with respect to claim 13 similar to its showing with respect to claim 1. *See, e.g.*, Pet. 13–26, 33.

Each of claims 6 and 8–10 depends directly from claim 1 and claim 11 depends directly from claim 10. We have reviewed Petitioner's showing with respect to dependent claims 6 and 8–11. For instance, with respect to claim 6's further recitation of a unit for combining the indication with a check signal, as Petitioner contends (*see, e.g.*, Pet. 24–26, 29–30), Humphrey teaches operation check logic 17 that combines by comparing an operation state bit from the memory module with a reference (compare logic 69) (Ex. 1008, 11:22–27; Fig. 3; Ex. 1003 ¶ 73). Additionally, with respect to claim 8's further recitation of a main bus error detection unit, as Petitioner contends (Pet. 22–24, 30), Humphrey teaches address error detection in the processor subsystem (Ex. 1008, 9:25–10:2). Petitioner also submits the Admitted Prior Art. Pet. 30 (citing Ex. 1001, 1:25–30; Ex. 1003 ¶ 80). The teachings of the Admitted Prior Art (*id.*) are consistent with Petitioner's contentions based on the record before us at this juncture.

We now turn to claims 10 and 11. Claim 10 further recites "wherein the circuit module is a dual in-line memory module (DIMM), wherein the circuit units are memory units, wherein the main bus is a memory main bus, and the sub-buses are memory sub-busses." Ex. 1001, 8:28–32. Claim 11 further recites "wherein the memory main bus is a command/address bus." Ex. 1001, 8:33–34. Consistent with Petitioner's contentions (Pet. 30–32) and as discussed above with respect to claim 1, Humphrey teaches dual port

access to memory system 11,[12] including buses that carry command and address data (e.g., buses 27, 29, 33, 39) and memory modules 21, each of which comprises semiconductor storage array 55 (Ex. 1008, Figs, 1, 2, 4:7–12, 7:23–10:32). Additionally, Humphrey teaches memory devices, such as memory system 11, memory module 21, semiconductor storage array 55 (*id.*) and Dr. Subramanian testifies DIMMs would have been known to a person having ordinary skill in the art (Ex. 1003 ¶¶ 19, 82). Also consistent with Petitioner's contentions (Pet. 30–32) the further recitations of claims 10 and 11 are found in the Admitted Prior Art (*see, e.g.*, Ex. 1001, 1:11–38, 1:41–43, 1:57–59, Figs. 1, 2).

With respect to claim 14, Patent Owner contends that claim 14 requires that the error signal be generated by the indication signal unit and the teachings of Humphrey relied upon by Petitioner pertain to a unit outside of memory module 21. Prelim. Resp. 35–42. Based on the record before us, we agree with Patent Owner that claim 14 requires a memory unit "consisting of a single integrated circuit memory chip" that receives "a check signal." Additionally, we agree with Patent Owner that based on the record before us, Petitioner has not identified teachings corresponding to this recitation because logic 17 relied upon by Petitioner (Pet. 27–28, 33–34) resides in the processor subsystem outside of memory module 21 (Ex. 1008,

[12] Humphrey describes components of Figure 1 as corresponding to components of Figure 34 of U.S. Patent No. 4,228,496 ("the '496 Patent") (Ex. 1008, 8:6–11), which is identified as describing a multiple processor system that incorporates Humphrey's memory system 11 (Ex. 1008, 7:9–11). According to Humphrey, however, its memory control system "is not restricted to use in such systems." Ex. 1008, 7:12–15.

Fig. 1) and, instead, receives the operation state bit from memory module 21 (*id.* at Fig. 3).

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of showing claims 6, 8, 10, 11, and 13 to be unpatentable in view of Humphrey alone.[13] However, we determine that Petitioner has not demonstrated a reasonable likelihood of showing claim 14 to be unpatentable in view of Humphrey.

7. Discussion of Claim 9

Petitioner asserts that Humphrey in combination with Cromer teaches all elements of claim 9 and provides a rationale for combining the teachings of Humphrey and Cromer. Pet. 34–36. As Petitioner contends (*id.*), Cromer teaches sticky bits for holding information (Ex. 1007 ¶¶ 1, 8, 11, 15, 16). Additionally, based on the record before us at this juncture, Petitioner's asserted reason for combining the teachings of Humphrey and Cromer (Pet. 34–36) has rational underpinning and is consistent with the teachings cited therein. Patent Owner does not argue separately Petitioner's contentions regarding claim 9.

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of

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[13] Based on the record before us at this juncture, the teachings of the Admitted Prior Art are consistent with and provide further support for Petitioner's contentions with respect to independent claim 13, and the further recitations of claims 8, 10, and 11.

showing claim 9 to be unpatentable in view of Humphrey in combination with Cromer.

8. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1, 6, 8, 10, 11 and 13 are unpatentable as obvious over Humphrey alone or in combination with the Admitted Prior Art. On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claim 9 is unpatentable as obvious over Humphrey and Cromer, together or also in combination with the Admitted Prior Art.

G. Obviousness of Claims 1, 6, 8–11, 13, and 14 over Raynham with other art

Petitioner contends claims 1, 10, 11, 13, and 14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Raynham and Seyyedy. Pet. 39–58. Petitioner also contends that claims 6, 8, and 9 are unpatentable under 35 U.S.C. § 103(a) as obvious over Raynham, Seyyedy, and other art, specifically, Humphrey (as to claim 6), Admitted Prior Art (as to claim 8), or Cromer (as to claim 9). *Id.* at 58–62.

1. Overview of Raynham

Raynham is directed to providing error detection and correction on the same chip as DRAM memory. Ex. 1005, Abstract. Figure 4 of Raynham is reproduced below.

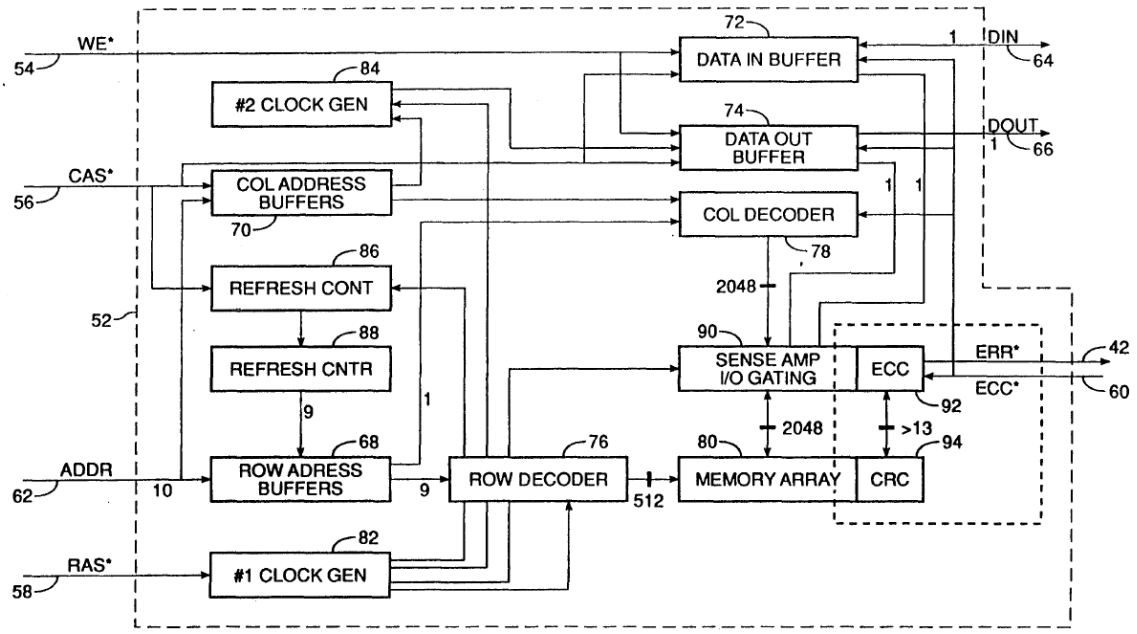

FIG. 4

Figure 4 is a block diagram of a DRAM.

DRAM chip 52 receives control signals and address signals on lines 54, 56, and 58, and error correction code signals on line 60. *Id.* at 5:16–21. These signals are used during the operation of error correction code (ECC) circuitry 92. *Id.* at 6:58–60.

2. Overview of Seyyedy

Seyyedy is directed to a memory module, such as a DIMM or a single inline memory module (SIMM), which incorporates error correction circuitry. Ex. 1009, Abstract. Figure 2 of Seyyedy is reproduced below.

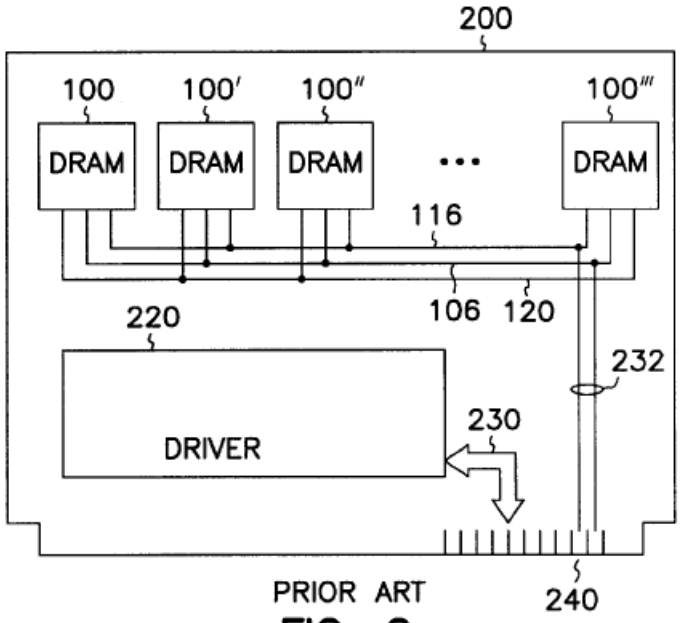

FIG. 2

Figure 2 is a block diagram of a conventional SIMM.

As shown above in Figure 2, the SIMM includes DRAMs 100–100‴ mounted on circuit board 200. *Id.* at 4:27–28. DRAMs 100–100‴ are integrated circuit chips that are mounted directly on circuit board 200 and environmentally encapsulated. *Id.* at 4:40–43.

3. Discussion of Claim 1

We begin our analysis with independent claim 1. Petitioner asserts that the combination of Raynham and Seyyedy teaches all elements of claim 1 and provides a rationale for combining the teachings of Raynham and Seyyedy. Pet. 39–52.

Claim 1 is directed to a circuit module, which comprises circuit units arranged on a module board and a main bus that branches into sub-buses, each of which is connected to one of the circuit units. Ex. 1001, 7:30–38. Petitioner points to Raynham's teachings relating to a memory subsystem, including DRAM memory array 50 comprised of DRAM chips 52, which

receive, through sub-buses, address and control information, as well as data conveyed on system bus 12. Pet. 44–49 (citing Ex. 1005, 3:48–63, 5:4–17, Figs. 1–4; Ex. 1003 ¶¶ 19, 97–101). Petitioner contends a person of ordinary skill in the art would understand DRAM chips 52 of DRAM memory array 50 would be arranged on a module board to enable connection, but Petitioner also points to Seyyedy's teachings of arranging such chips on a circuit board and encapsulating memory devices. Pet. 45–46 (citing Ex. 1009, 2:37–38, 2:46–52, Figs. 2, 3; Ex. 1003 ¶¶ 19, 98, 100). Petitioner additionally points to Seyyedy's teachings of communication lines and buses as further evidence that it would have been known to a person of ordinary skill in the art to use a main bus branching into a plurality of sub-buses to connect memory devices within a computer system. Pet. 49 (citing Ex. 1009, 4:39–40, Fig. 2; Ex. 1003 ¶ 104).

Consistent with Petitioner's contentions, Raynham teaches a computer system that includes a memory subsystem that receives control, data, and address signals over high-speed system bus 12. Ex. 1005, 3:48–64. Also consistent with Petitioner's contentions, Raynham teaches that the memory subsystem includes DRAM memory array 50, which comprises DRAM chips 52 that receive the control, data, and address signals. *Id.* at 5:4–22, Figs. 3–5. Furthermore, Seyyedy teaches a "circuit board" (Ex. 1009, 2:36–38), as well as providing "memories which are directly mounted on the printed circuit board and environmentally encapsulated" (*id.* at 2:46–52). As Petitioner contends (Pet. 49), Seyyedy teaches bi-directional data communication line that communicates with DRAM devices 100–100''' mounted on circuit board 200 (Ex. 1009, 4:27–28, 4:38–45).

Claim 1 also recites that each circuit unit comprises an indication signal generating unit, which provides an indication signal based on a combination of signals received on the sub-buses. Ex. 1001, 7:39–44. Petitioner points to Raynham's teachings relating to providing error detection and correction on DRAM chip 52. Pet. 50–52 (citing Ex. 1005, 2:55–63, 6:58–60, 7:3–25, Figs. 4, 5; Ex. 1003 ¶¶ 105–107). Consistent with Petitioner's contentions (*id.*), Raynham teaches an error correction code (ECC) checking and generating circuit formed on each chip (Ex. 1005, 5:7–9) that, using incoming data (*id.* at 6:58–60), detects the presence of errors in the data bits (*id.* at 7:2–25).

Petitioner also provides reasons to combine the teachings of Raynham and Seyyedy. Pet. 39–44 (citing Ex. 1005, 3:22–27, 5:4–17, 7:14–16, 7:23–25, Figs. 3, 4; Ex. 1009, 2:36–37, 2:46–52; Ex. 1008, 2:17–27, 3:17–20; Ex. 1006, Abstract; Ex. 1003 ¶¶ 49–52). For instance, relying on the testimony of Dr. Subramanian, Petitioner contends that the skilled artisan would have had a reason to combine the teachings of the asserted art to improve the memory system by generating the status on the chip itself to avoid bottlenecks and improve memory access time. *Id.* at 43 (citing Ex. 1005, 3:22–27; Ex. 1003 ¶¶ 49–52). Petitioner also characterizes the proposed combination of teachings as "an application of a known technique to a known device," and further characterizes on-chip error detection as "well known." Pet. 43–44 (citing Ex. 1005, 3:22–27; Ex. 1008, 2:17–27, 3:17–20; Ex. 1006, Abstract; Ex. 1003 ¶¶ 49–52).

Patent Owner contends that Petitioner has not shown that a person of ordinary skill in the art would have had a reason to combine the teachings of Raynham and Seyyedy. Prelim. Resp. 43. Patent Owner, more specifically,

contends that Raynham teaches error correction for data stored in a module, whereas Seyyedy teaches against including any error correction on individual DRAM devices. *Id.* at 45–47. Patent Owner asserts that, therefore, Seyyedy teaches away from Petitioner's proposed combination. *Id.* at 47–49.

Based on the record before us at this juncture, we find that Seyyedy does not criticize, discredit, or otherwise discourage the use of mounting memory on a circuit board and receiving signals from a main bus with Raynham's providing error detection and correction on a DRAM chip. *See DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) ("A reference does not teach away, however, if it merely expresses a general preference for an alternative invention but does not 'criticize, discredit, or otherwise discourage' investigation into the invention claimed.") (*quoting In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)). Seyyedy's illustration of ECC 300 in driver 220 (Ex. 1009, Fig. 3) to "eliminate the need for an additional component" (*id.* at 5:29–31) does not criticize, discredit, or otherwise discourage the use of providing error correction on the DRAM devices. Instead, Seyyedy teaches that error correction technology solves the problem of increased expense of manufacturing memory devices without defects. *Id.* at 5:23–28. Seyyedy also provides multiple embodiments including that shown in Figure 3 incorporating error correction in "a common package" (*id.* at 5:31) and an alternate embodiment in which error correction is provided "as a separate packaged component" (*id.* at 5:55–56).

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we

determine that Petitioner has demonstrated a reasonable likelihood of showing claim 1 to be unpatentable in view of Raynham and Seyyedy.

4. Discussion of claims 8, 10, 11, 13, and 14

Turning now to independent claim 13 and dependent claims 8, 10, 11, and 14, Petitioner asserts that the combination of Raynham and Seyyedy teaches all elements of these claims and provides a rationale for combining the teachings of Raynham and Seyyedy. Pet. 39–62. Patent Owner does not argue these claims separately, except as otherwise noted herein. Independent claim 13 is similar to claim 1. Based on the record before us and at this juncture, Petitioner has made a sufficient showing with respect to claim 13 similar to its showing with respect to claim 1. *See, e.g.*, Pet. 39–52, 56.

Claim 8 depends directly from claim 1 and further recites a main bus error detection unit. Consistent with Petitioner's contentions (Pet. 42–46), Seyyedy teaches incorporating error correction circuitry in a memory module, such as a DIMM (Ex. 1009, Abstract, Figs. 2, 3). Seyyedy also teaches that "[l]ocating error correction circuitry 300 at the point of message transmission into or out of memory module 200 provides error-free output even when the memory devices 100 do not have all memory cells functional." *Id.* at 5:34–38, Fig. 3. Additionally, Petitioner submits the Admitted Prior Art. Pet. 60 (citing Ex. 1001, 1:25–31; Ex. 1003 ¶ 122). The teachings of the Admitted Prior Art (*id.*) are consistent with Petitioner's contentions based on the record before us at this juncture.

Claim 10 depends directly from claim 1 and claim 11 depends from claim 10. Claim 10 further recites that the circuit module is a dual in-line memory module, the circuit units are memory units, the main bus is a

memory main bus, and the sub-buses are memory sub-buses. Ex. 1001, 8:28–32. Consistent with Petitioner's contentions (Pet. 55), Seyyedy teaches that "DIMMs (dual in-line memory modules)" may be integrated "in the same fashion" as SIMM devices (DRAM devices 100–100'"). Ex. 1009, 4:47–50; *see also* Ex. 1003 ¶ 112 ("One of normal skill in the art would understand that the memory system of Raynham could be implemented on a known memory configuration, such as the DIMM described by Seyyedy, because to do so merely represents an application of a known technique to a known device."). Also, consistent with Petitioner's contentions with respect to claims 1 and 10 (Pet. 44–49, 54–56), Raynham teaches that the buses are memory buses (*see, e.g.*, Ex. 1005, Figs. 3, 4).

Claim 11 further recites that the memory main bus is a command/address bus. Ex. 1001, 8:33–34. Consistent with Petitioner's contentions (Pet. 48, 49, 55, 56), Raynham teaches receiving command and address signals over the main bus (Ex. 1005, Figs. 1, 3, 4).

We have also reviewed Petitioner's showing with respect to claim 14. Claim 14 depends from independent claim 13 and further recites that the memory unit comprises a check signal input and the indication signal generation unit generates the indication signal using the check signal, as well as the combination of signals received on the memory bus. Ex. 1001, 8:48–54. Petitioner points to Raynham's teaching of an ECC enable signal and use of that signal by the on-chip error correction circuitry, for example, as illustrated in Figure 5. Pet. 57–58 (citing Ex. 1005, 5:16–21, 6:58–60, 7:9–25, Figs. 4, 5; Ex. 1003 ¶¶ 119, 120).

Patent Owner contends that the "'check signal' must contain content such as parity data that is used to 'check' whether the data contains any

error," whereas the signal identified by Petitioner "is merely a control signal that determines the timing of error correction." Prelim. Resp. 50–51 (citing Ex. 1001, 5:29–42). Consistent with Petitioner's contentions, however, Raynham teaches that DRAM chip 52 "receives control signals via a write-enable (WE) line 54, a column address strobe (CAS) line 56, a row address strong (RAS) line 58, and an error correction code (ECC) line 60" (Ex. 1005, 5:16–20) and that "CRC bits are used in connection with correcting 2048 data bits" (*id*. at 6:29–30). Petitioner points to the timing diagram in support of its contention that these signals are received and used. Pet. 57–58.

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of showing claims 8, 10, 11, 13, and 14 to be unpatentable in view of Raynham and Seyyedy.

5. Discussion of claims 6 and 9

Petitioner asserts that Raynham and Seyyedy in combination with either Humphrey or Cromer teach all elements of claims 6 and 9, respectively, and provides a rationale for combining the teachings of the asserted art. Pet. 58–62. Petitioner relies on the same portions of Humphrey and Cromer (*id.*) previously discussed and we find Petitioner's contentions sufficient for institution for the reasons given above. Additionally, based on the record before us at this juncture, Petitioner's asserted reasons for combining the teachings of the asserted art (Pet. 58–61) have rational underpinning and are consistent with the teachings cited therein. Patent

Owner does not argue separately Petitioner's contentions regarding claims 6 and 9.

Having reviewed the Petition and Preliminary Response, and the evidence cited therein, based on the record before us at this juncture, we determine that Petitioner has demonstrated a reasonable likelihood of showing claim 6 to be unpatentable in view of Raynham, Seyyedy, and Humphrey. We also determine that Petitioner has demonstrated a reasonable likelihood of showing claim 9 to be unpatentable in view of Raynham, Seyyedy, and Cromer.

6. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1, 10, 11, 13 and 14 are unpatentable as obvious over Raynham and Seyyedy. On this record, we also are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 6 and 9 are unpatentable as obvious over Raynham, Seyyedy and Humphrey or Cromer, respectively. On this record, we further are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claim 8 is unpatentable as obvious over Raynham and Seyyedy together, or also in combination with the Admitted Prior Art.

III. CONCLUSION

For the foregoing reasons, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claims 1, 6, 8–11, 13, and 14 of the '978 Patent are unpatentable. We, however, determine that Petitioner has not made a

sufficient showing with respect to claims 2–5 and 12. At this preliminary stage, we have not made a final determination with respect to the patentability of the challenged claims or any underlying factual and legal issues.

IV. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1, 6, 8–11, 13, and 14 of the '978 Patent on the following grounds of unpatentability:

Reference(s)	**Basis**	**Challenged Claim(s)**
Humphrey alone or with the Admitted Prior Art	§ 103(a)	1, 6, 8, 10, 11, and 13
Humphrey and Cromer, together or also with the Admitted Prior Art	§ 103(a)	9
Raynham and Seyyedy	§ 103(a)	1, 10, 11, 13, and 14
Raynham, Seyyedy, and Humphrey	§ 103(a)	6
Raynham and Seyyedy, together or also with the Admitted Prior Art	§ 103(a)	8
Raynham, Seyyedy, and Cromer	§ 103(a)	9

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision; and

FURTHER ORDERED that the trial is limited to the grounds identified immediately above, and no other ground is authorized.

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